REMARKS

A timely filed Request For Continued Examination in compliance with 37 CFR 1.114 is filed concurrently herewith. Claims 1-16 are pending in the application and are finally rejected by Final Office Action mailed February 11, 2004. Claims 1-16 are canceled and new claims 17-31 are presented.

Final Rejections under 35 USC 103(a)

Claims 1-3, 6, 9-11 and 14 are under final rejection as being obvious over Maturi et al ("Maturi") in view of Fujii et al US 5898695 ("Fujii 1"). Claims 4-5 and 12-13 are finally rejected as being obvious over Maturi in view of Fujii 1 and further in view of Fujii et al US 6477179 ("Fujii 2"). It is respectfully submitted that new claims 17-31 avoid these rejections.

New independent claim 17 is directed to a method of processing a transport stream wherein each program identifier of an elemental stream is used to assign the stream a direct memory access (DMA) channel which is associated with a specific memory location of a host computer, and then the DMA transfers of the streams are performed using the DMA channels without being controlled by the microprocessor of the host computer.

The microprocessor of the host computer is involved with the stream transfers in both Maturi and Fujii 1. In Maturi, a host microcontroller 18 interacts with the decoder 16 via an arrangement of interrupts (e.g. see col. 4, lines 53-60; col. 6, lines 1-19) and does not disclose DMA transfers of the elementary streams. In Fujii 1, the interface unit 14 transfers all transport stream (TS) packet data to a packet landing buffer 71 in main memory RAM 7 in response to a interrupt signal from microprocessor 12 (e.g. see col. 6, lines 10-13). As disclosed, for example, in Figs. 5 and 14 of Fujii 1 and the associated text found at col. 6, lines 28-65 and col. 9, line 10-col. 10, line 16, respectively, microprocessor 12 controls the packet landing time and write address of the data transferred from interface unit 14 to packet landing buffer 71. The write timing of the transfer of packet data from transfer buffer 141 to the write address determined by microprocessor 12 in packet landing buffer 71 is controlled through a handshake with DMA controller 121 within microprocessor 12. Therefore, although Fujii 1 performs DMA transfers of

the multiple elementary streams from local memory to corresponding transfer locations in the host memory as stated by the examiner in the Final Office Action, this transfer is controlled by the microprocessor of the host computer. This element distinguishes new claims over Maturi and Fujii 1, alone or in combination. Fujii 2 was cited to show the elements of integrating a network interface connected to a network computer and connecting a personal computer to a service provider of the Internet, and does not change the above-stated conclusion of non-obviousness.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

Mart C. Matthews
Reg. No. 26,201

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (303) 571-4000
Fax: (303) 571-4321
MCM/cl
60199267 v1